

Diseño del Frente Digital de un Transceiver BPL

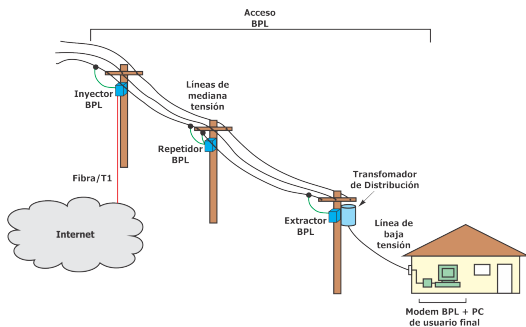
Paola Pezoimburu

Directora: Dra. Ing. Cecilia Galarza

Laboratorio de Procesamiento de Señales y Comunicaciones

11 de agosto de 2010

Broadband over Power Lines



Tipo de Transmisión	Frec. de Transmisión
Radio AM	530-1600 KHz
Radio FM	88-108 MHz
VHF TV	178-216 MHz
Radio Celular	850 MHz
Indoor Wireless Networks	1.8GHz
Satellite Downlink	3.7-4-2 GHz
Satellite Uplink	5.9-6.4 GHz
Fibra Óptica	2×10^{14} Hz
BPL	1-30 MHz

PLC:

Open PLC European

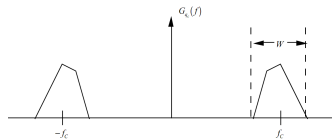
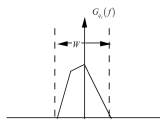
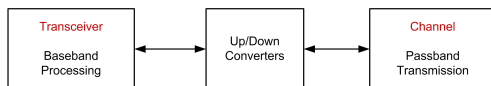
Research Alliance (OPERA).

BPL:

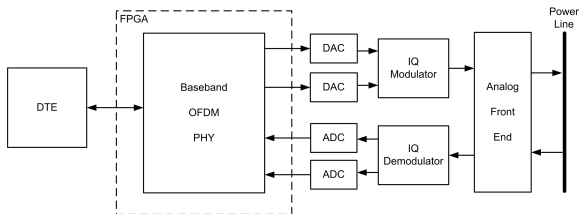
Institute of Electrical

and Electronics Engineers (IEEE).

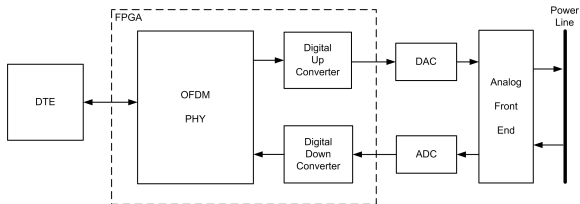
Up/Down Conversion



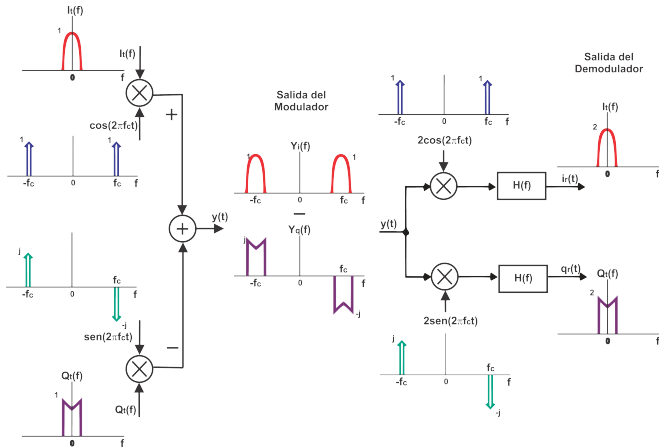
Analog Up/Down Conversion

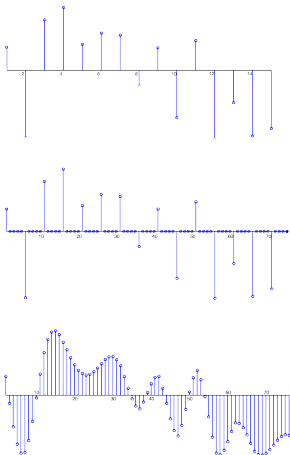


Digital Up/Down Conversion



Modulación/Demodulación IQ

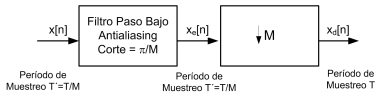




Interpolación



Decimación



Descomposiciones Polifásicas Equivalentes

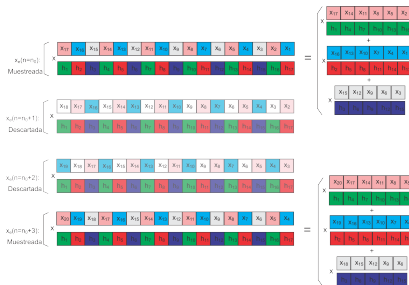
Interpolación

$$\begin{matrix} n(n): \\ \begin{matrix} x_p(n) \\ x \\ h(n) \end{matrix} \end{matrix} \begin{matrix} \begin{matrix} 0 & 0 & x_0 & 0 & 0 & 0 & 0 & 0 & x_1 & 0 & 0 & 0 & 0 & x_2 \end{matrix} \\ \begin{matrix} x_0 & x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 & x_9 & x_{10} & x_{11} & x_{12} & x_{13} \end{matrix} \end{matrix} = \begin{matrix} \begin{matrix} x(n) \\ x \\ h(n) \end{matrix} \end{matrix} \begin{matrix} \begin{matrix} x_0 & x_1 & x_2 & x_3 \end{matrix} \\ \begin{matrix} x_4 & x_5 & x_6 & x_7 \end{matrix} \end{matrix}$$

$$\begin{matrix} n(n)+1 \\ \begin{matrix} x_p(n) \\ x \\ h(n) \end{matrix} \end{matrix} \begin{matrix} \begin{matrix} x_0 & 0 & 0 & x_1 & 0 & 0 & x_2 & 0 & 0 & x_3 & 0 & 0 & 0 & x_4 \end{matrix} \\ \begin{matrix} x_0 & x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 & x_9 & x_{10} & x_{11} & x_{12} & x_{13} \end{matrix} \end{matrix} = \begin{matrix} \begin{matrix} x(n) \\ x \\ h(n) \end{matrix} \end{matrix} \begin{matrix} \begin{matrix} x_0 & x_1 & x_2 & x_3 & x_4 \end{matrix} \\ \begin{matrix} x_5 & x_6 & x_7 & x_8 & x_9 \end{matrix} \end{matrix}$$

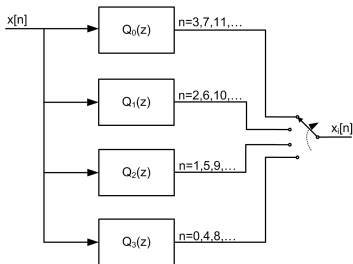
$$\begin{matrix} n(n)+2 \\ \begin{matrix} x_p(n) \\ x \\ h(n) \end{matrix} \end{matrix} \begin{matrix} \begin{matrix} 0 & x_0 & 0 & 0 & x_1 & 0 & 0 & x_2 & 0 & 0 & x_3 & 0 & 0 & 0 & x_4 \end{matrix} \\ \begin{matrix} x_0 & x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 & x_9 & x_{10} & x_{11} & x_{12} & x_{13} \end{matrix} \end{matrix} = \begin{matrix} \begin{matrix} x(n) \\ x \\ h(n) \end{matrix} \end{matrix} \begin{matrix} \begin{matrix} x_0 & x_1 & x_2 & x_3 & x_4 \end{matrix} \\ \begin{matrix} x_5 & x_6 & x_7 & x_8 & x_9 \end{matrix} \end{matrix}$$

Decimación

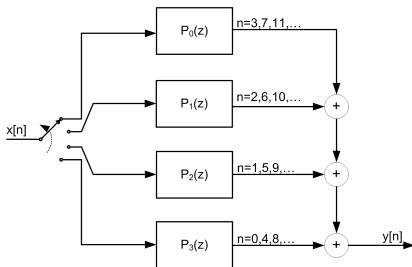


Descomposiciones Polifásicas Equivalentes

Interpolación

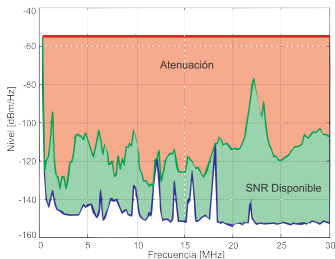


Decimación



Medidas de Performance

Canal de Transmisión



Mean Square Error:

$$MSE = \frac{1}{M \cdot N} \cdot \sum_{k=1}^{M \cdot N} |S(k) - S_0(k)|^2$$

Error Vector Magnitude:

$$\Rightarrow EVM = \sqrt{\frac{\frac{1}{M \cdot N} \cdot \sum_{k=1}^{M \cdot N} |S(k) - S_0(k)|^2}{\frac{1}{M \cdot N} \cdot \sum_{k=1}^{M \cdot N} |S_0(k)|^2}} \cdot 100 \%$$

Signal-to-Noise Ratio:

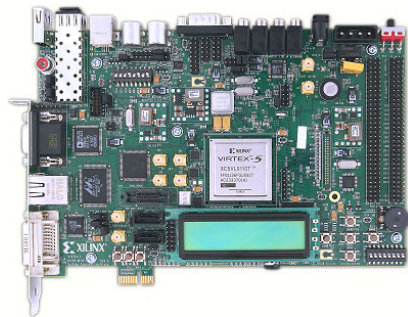
$$SNR = 10 \cdot \log_{10} \left(\frac{\frac{1}{K} \sum |x[n]|^2}{\frac{1}{K} \sum e[n]^2} \right) [dB]$$

Plataforma física: Field-Programmable Gate Array (FPGA)

Xilinx provee amplias
herramientas de diseño

Virtex-5 OpenSPARC Evaluation
Platform

Xilinx Virtex®-5 XC5VLX110T



Herramienta de diseño y simulación: Xilinx System Generator for DSP

Corre sobre *Simulink* agregando sets de bloques propios.

Genera automáticamente, a partir del sistema construido, el código en VHDL.

Permite integrar al sistema scripts generados en *Matlab*, y admite importar y exportar datos a su workspace.

