Implementación de un Sistema de Modulación Wavelet Multiportadora

Tesis de Grado

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LPSC
Laboratorio de Procesamiento de Señales y Comunicaciones

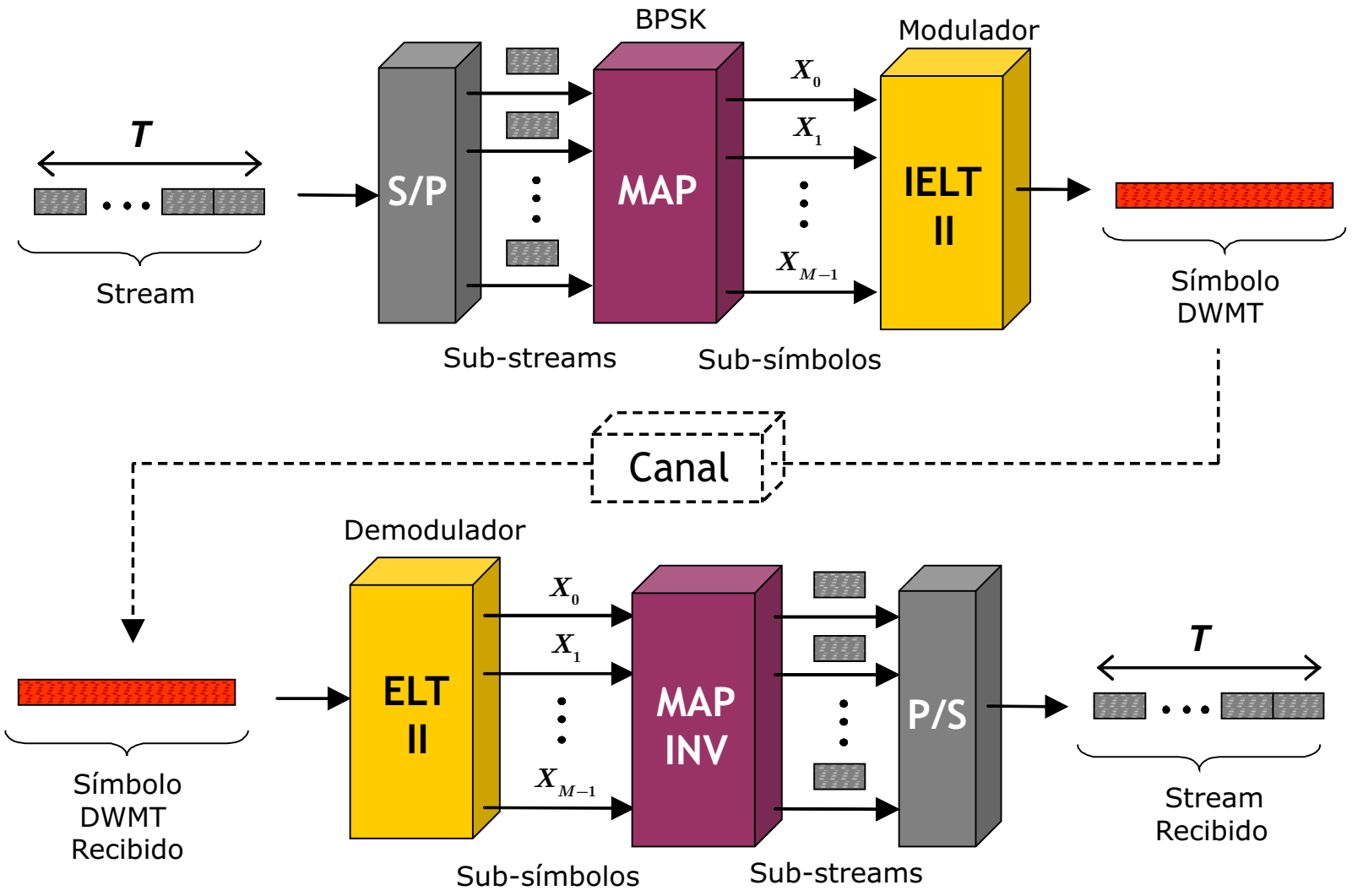
Objetivos

- Proponer un esquema de *Modulación Wavelet Multiportadora* para un sistema de comunicación BPL.

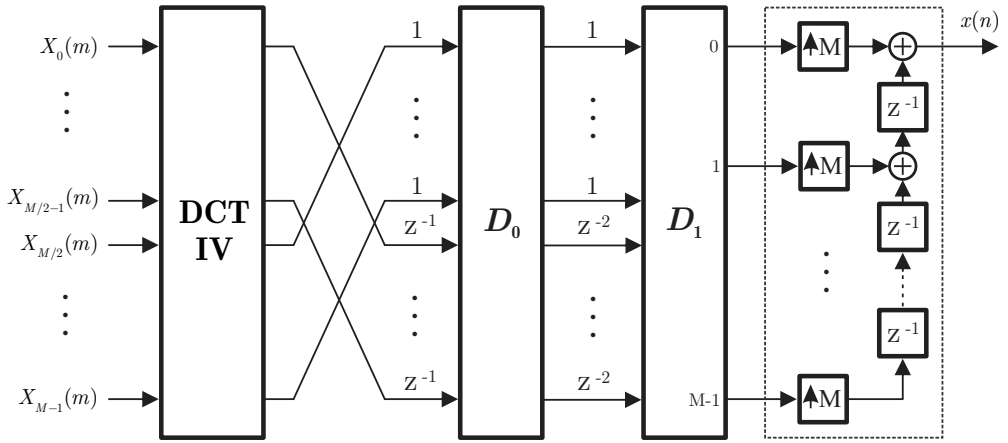
- Elvaluar los algoritmos más eficientes para su implementación.

- Diseñar una descripción de hardware para implementar los algoritmos elegidos sobre una FPGA.

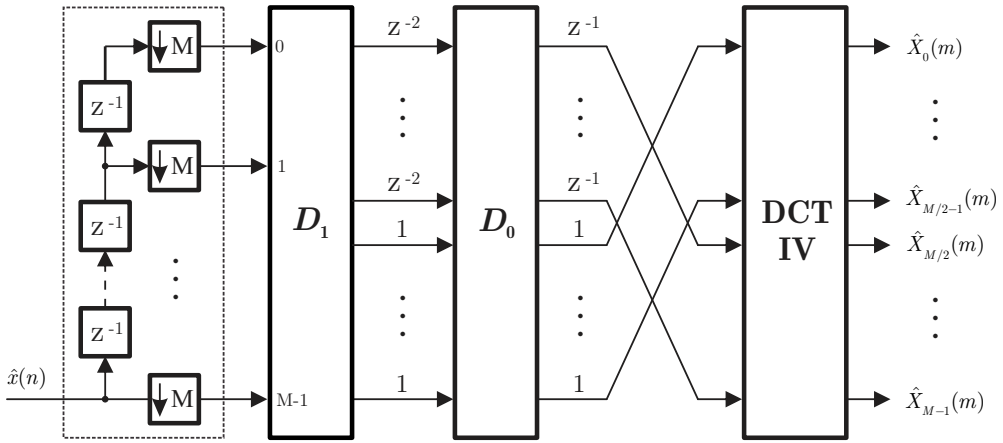
Esquema de Modulación DWMT-ELT-II



Extended Lapped Transform type-II (ELT-II)



IELT-II
Transformada inversa de *M* puntos



ELT-II
Transformada directa de *M* puntos

Etapas D_0 y D_1

Matriz D_j (*para j={0,1}, M=8*)

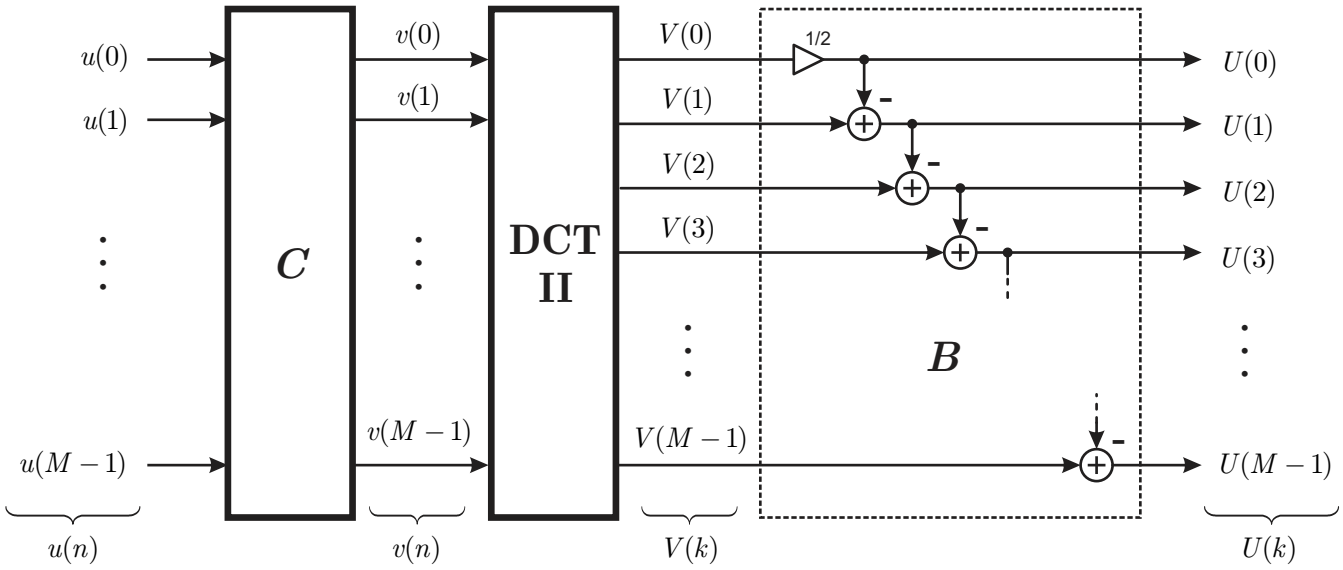
$$D_j = \begin{bmatrix} -\cos(\theta_{0,j}) & 0 & 0 & 0 & 0 & 0 & 0 & \sin(\theta_{0,j}) \\ 0 & -\cos(\theta_{1,j}) & 0 & 0 & 0 & 0 & \sin(\theta_{1,j}) & 0 \\ 0 & 0 & -\cos(\theta_{2,j}) & 0 & 0 & \sin(\theta_{2,j}) & 0 & 0 \\ 0 & 0 & 0 & -\cos(\theta_{3,j}) & \sin(\theta_{3,j}) & 0 & 0 & 0 \\ 0 & 0 & 0 & \sin(\theta_{3,j}) & \cos(\theta_{3,j}) & 0 & 0 & 0 \\ 0 & 0 & \sin(\theta_{2,j}) & 0 & 0 & \cos(\theta_{2,j}) & 0 & 0 \\ 0 & \sin(\theta_{1,j}) & 0 & 0 & 0 & 0 & \cos(\theta_{1,j}) & 0 \\ \sin(\theta_{0,j}) & 0 & 0 & 0 & 0 & 0 & 0 & \cos(\theta_{0,j}) \end{bmatrix}$$

Factores de fase

$$\theta_{i,0} = -\left((2i+1)\frac{1}{M} + 3\right)\frac{\pi}{8} \qquad \theta_{i,1} = \left((2i+1)\frac{1}{M} - 3\right)\frac{\pi}{8}$$

Discrete Cosine Transform type-**IV** (DCT-IV)

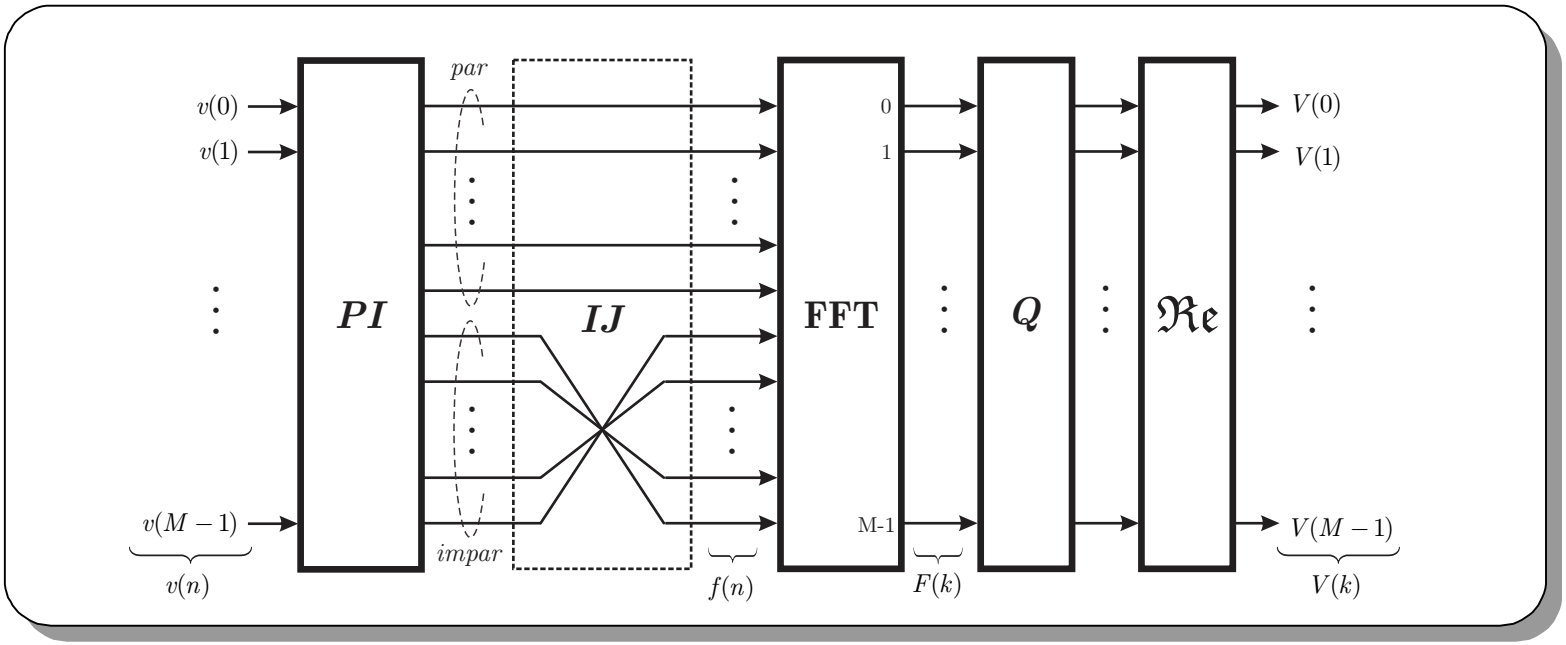
$$U(k) = \sum_{n=0}^{M-1} u(n) \cos\left[\frac{\pi}{M}\left(k+\frac{1}{2}\right)\left(n+\frac{1}{2}\right)\right] \qquad \begin{cases} k=0,1,\ldots,M\text{-}1 \\ n=0,1,\ldots,M\text{-}1 \end{cases}$$



$$C = 2diag\left\{c(0), c(1), \ldots, c(M-1)\right\} \qquad c(n) = \cos\left[\frac{\pi}{2M}\left(n+\frac{1}{2}\right)\right]$$

Discrete Cosine Transform type-II (DCT-II)

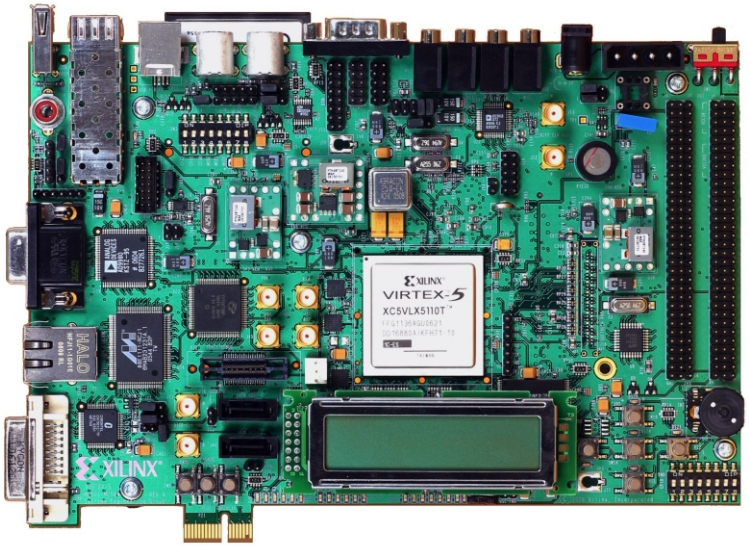
$$V(k) = \sum_{n=0}^{M-1} v(n) \cos\left[\frac{\pi}{M}\left(n+\frac{1}{2}\right)k\right] \qquad \begin{cases} k=0,1,\ldots,M\text{-}1 \\ n=0,1,\ldots,M\text{-}1 \end{cases}$$



$$Q = diag\left\{q(0), q(1), \ldots, q(M-1)\right\} \qquad q(k) = \cos\left(\tfrac{\pi}{2M}k\right) - j\sin\left(\tfrac{\pi}{2M}k\right)$$

Plataforma física elegida

Virtex-5 XC5VLX110T de Xilinx



Características del kit:

1GB Compact Flash card

256 MB SODIMM module

SATA cable

XUP USB-JTAG

Programming Cable

DVI to VGA adaptor

6A power supply.

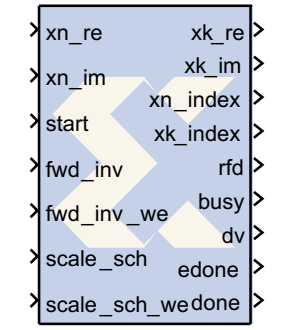
Justificación de la elección

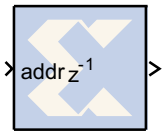
- Dispositivo reprogramable.
- Procesamiento de alta velocidad.
- Mayor control de las interfaces entre el dispositivo y los DAC/ADC.

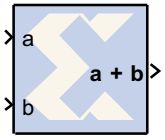
Herramienta de diseño

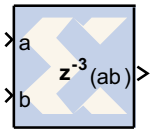
XILINX SYSTEM GENERATOR™ For DSP

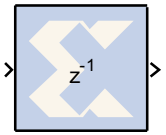
MATLAB® SIMULINK®





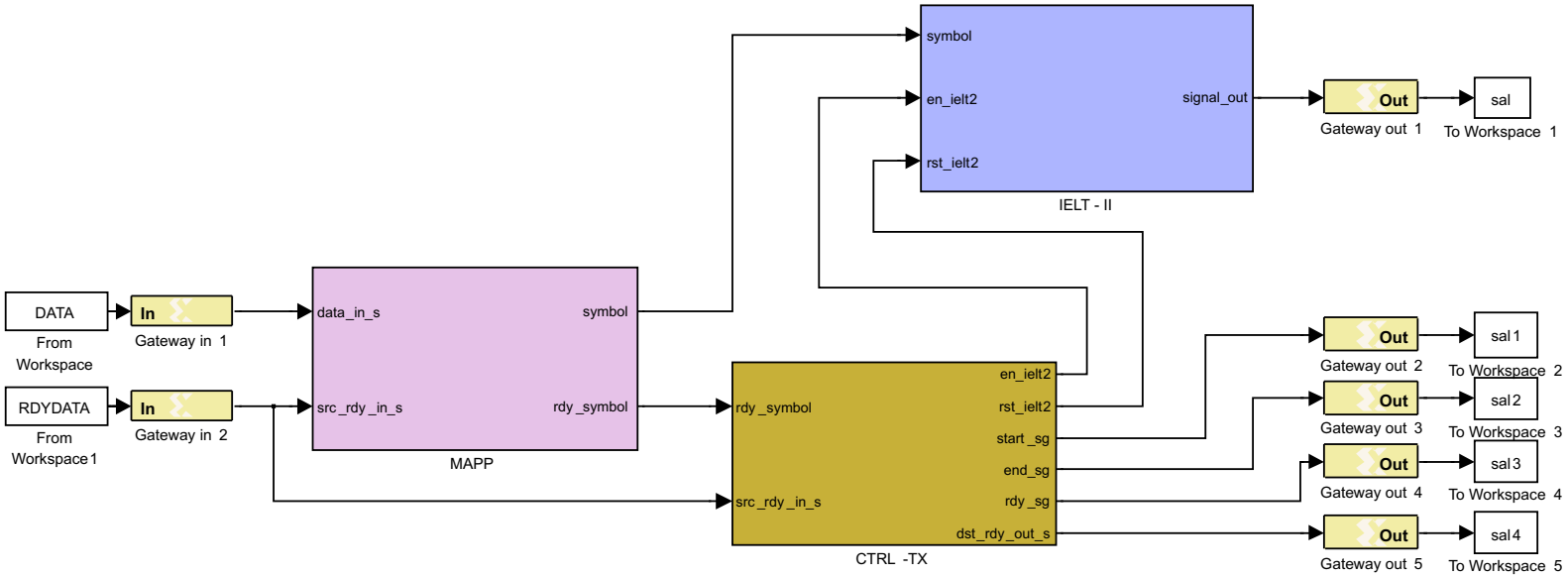


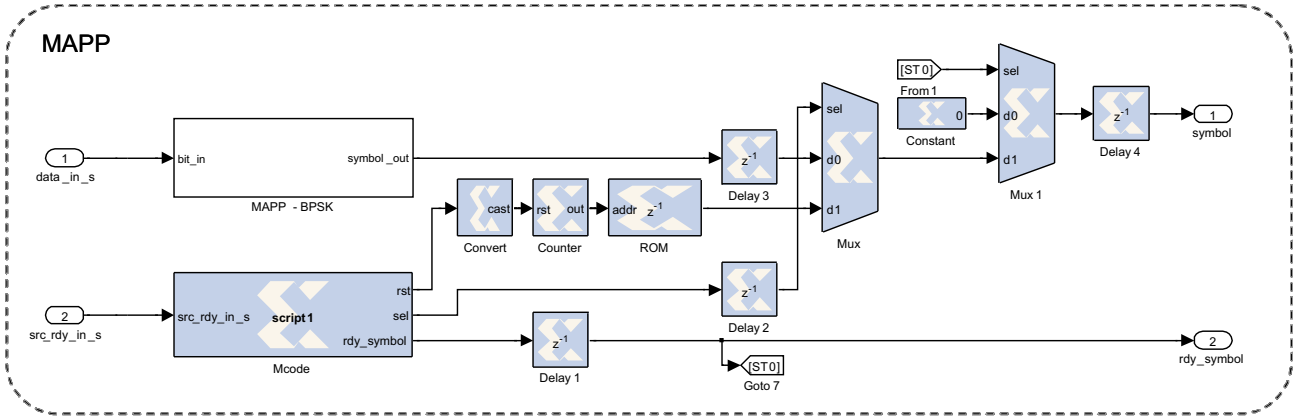




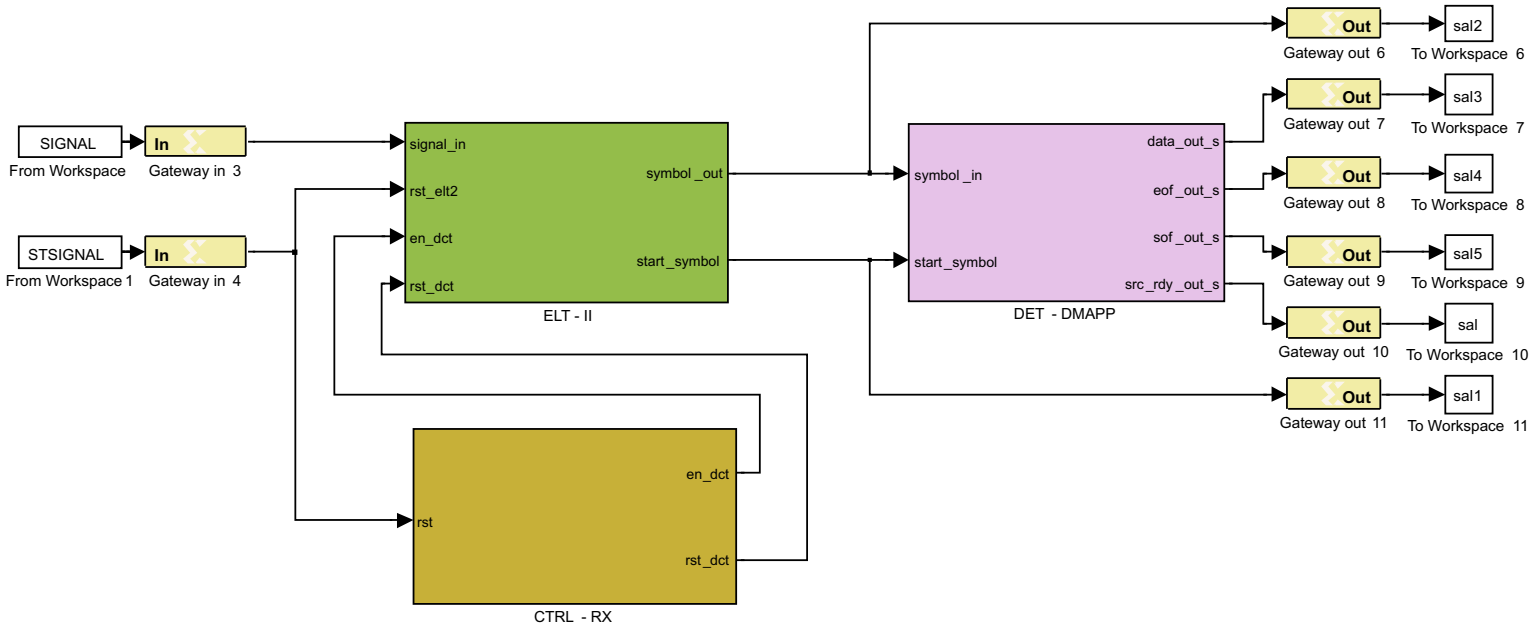
- Herramienta de alto nivel para el diseño de sistemas de procesamiento digital de alta performance utilizando FPGAs.
- Entorno de diseño en Simulink.

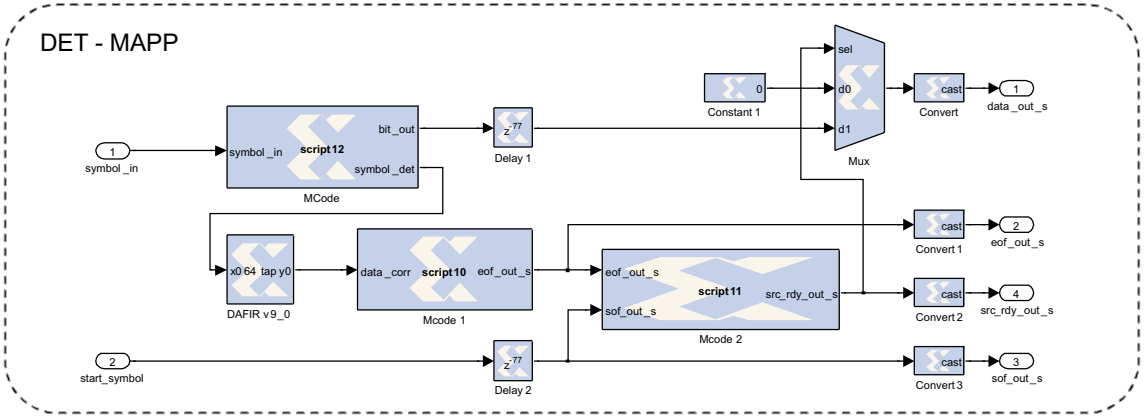
Transmisor


symbol
en_ielt2
rst_ielt2
signal_out
IELT - II
Out
Gateway out 1
sal
To Workspace 1
DATA
From Workspace
In
Gateway in 1
RDYDATA
From Workspace1
In
Gateway in 2
data_in_s
src_rdy_in_s
symbol
rdy_symbol
MAPP
rdy_symbol
src_rdy_in_s
en_ielt2
rst_ielt2
start_sg
end_sg
rdy_sg
dst_rdy_out_s
CTRL -TX
Out
Gateway out 2
sal1
To Workspace 2
Out
Gateway out 3
sal2
To Workspace 3
Out
Gateway out 4
sal3
To Workspace 4
Out
Gateway out 5
sal4
To Workspace 5

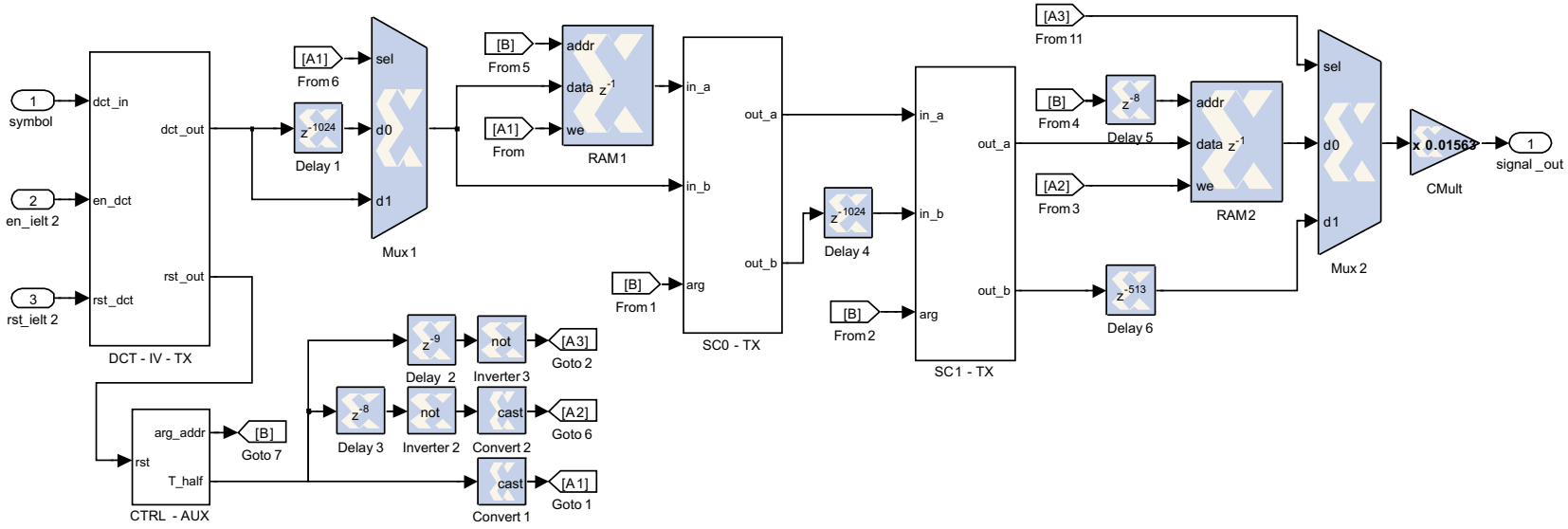

MAPP
1
data_in_s
bit_in
symbol_out
MAPP - BPSK
2
src_rdy_in_s
src_rdy_in_s
script1
rst
sel
rdy_symbol
Mcode
cast
Convert
rst
out
Counter
addr
ROM
Delay 3
Delay 2
Delay 1
sel
d0
d1
Mux
[ST0]
From 1
0
Constant
sel
d0
d1
Mux 1
Delay 4
1
symbol
2
rdy_symbol
[ST0]
Goto 7

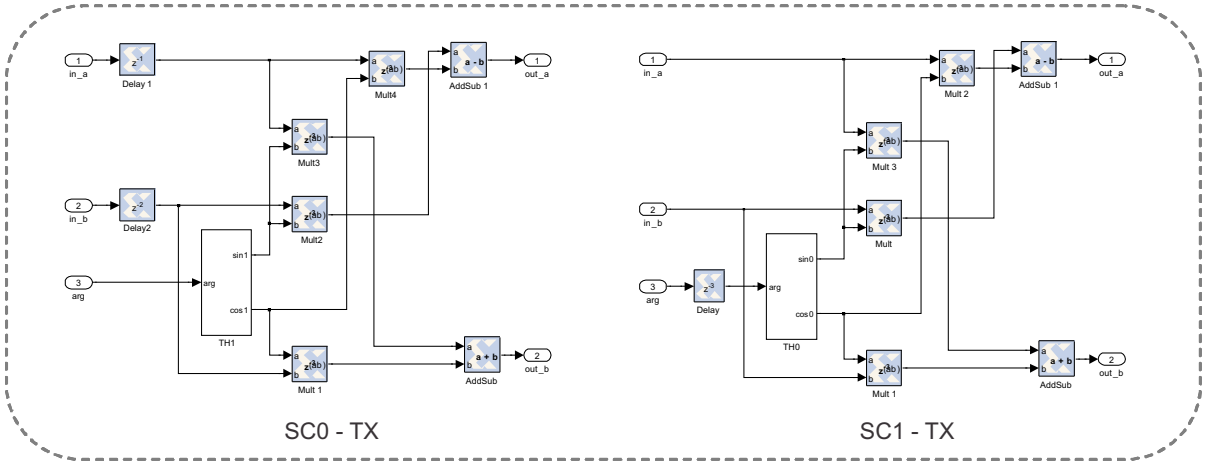
Receptor


SIGNAL
From Workspace
In
Gateway in 3
STSIGNAL
From Workspace 1
In
Gateway in 4
signal_in
rst_elt2
en_dct
rst_dct
symbol _out
start_symbol
ELT - II
symbol _in
start_symbol
data_out_s
eof _out_s
sof _out_s
src_rdy _out_s
DET - DMAPP
Out
Gateway out 6
sal2
To Workspace 6
Out
Gateway out 7
sal3
To Workspace 7
Out
Gateway out 8
sal4
To Workspace 8
Out
Gateway out 9
sal5
To Workspace 9
Out
Gateway out 10
sal
To Workspace 10
Out
Gateway out 11
sal1
To Workspace 11
rst
en_dct
rst_dct
CTRL - RX

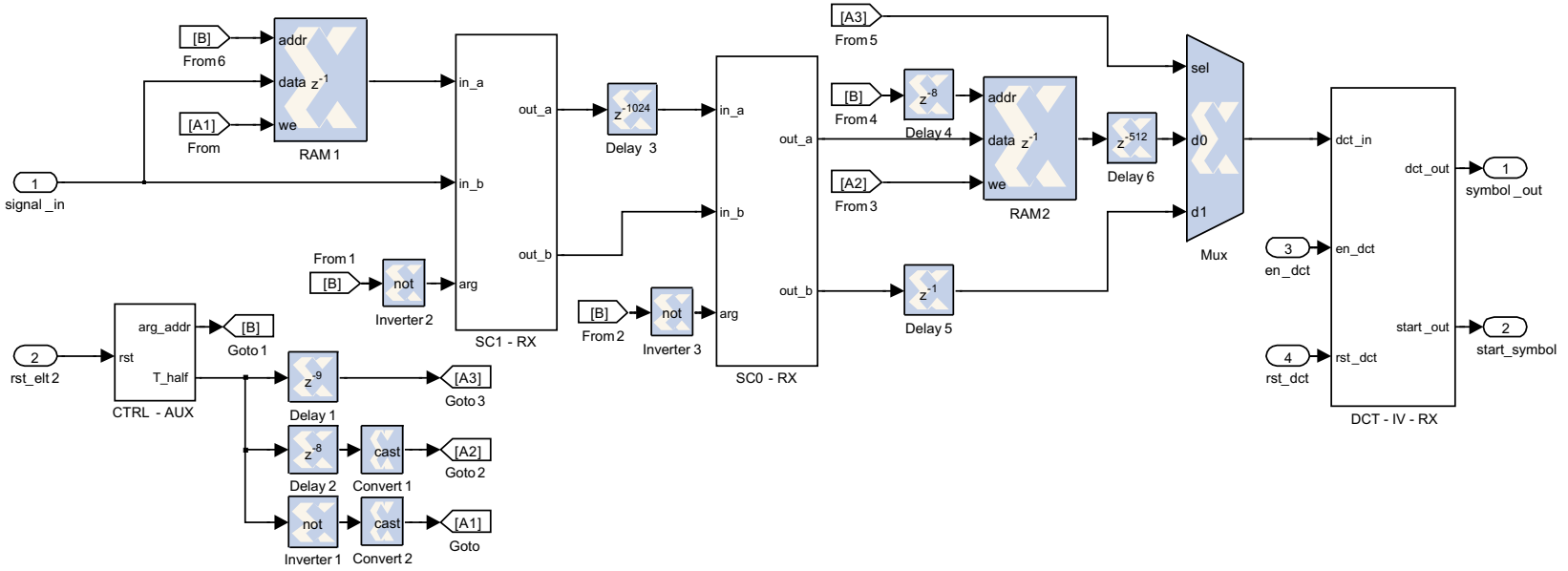

DET - MAPP
1
symbol _in
symbol _in
script12
bit _out
symbol _det
MCode
Delay 1
0
Constant 1
sel
d0
d1
Mux
cast
Convert
1
data _out _s
x0 64 tap y0
DAFIR v9_0
data _corr
script10
eof _out _s
Mcode 1
eof _out _s
sof _out _s
script11
src_rdy_out _s
Mcode 2
cast
Convert 1
2
eof _out _s
cast
Convert 2
4
src_rdy_out _s
2
start_symbol
Delay 2
cast
Convert 3
3
sof _out _s

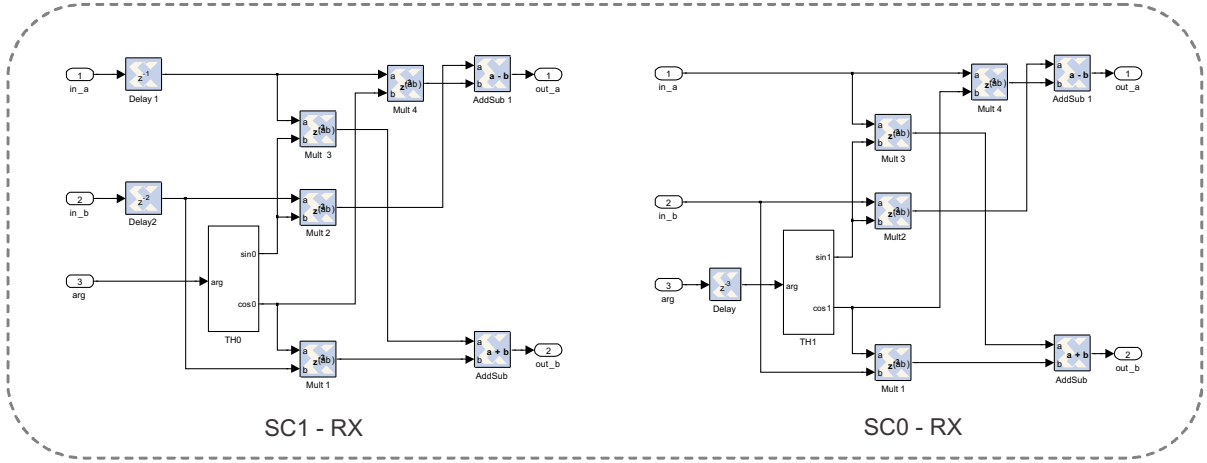
IELT-II


1
symbol
2
en_ielt 2
3
rst_ielt 2
dct_in
en_dct
rst_dct
dct_out
rst_out
DCT - IV - TX
[A1]
From 6
sel
d0
d1
Mux 1
Delay 1
[B]
From 5
addr
data
we
RAM 1
[A1]
From
in_a
in_b
arg
out_a
out_b
SC0 - TX
[B]
From 1
Delay 4
[B]
From 2
SC1 - TX
[A3]
From 11
[B]
From 4
Delay 5
[A2]
From 3
RAM 2
Mux 2
x 0.01563
CMult
signal _out
Delay 6
Delay 2
Inverter 3
Goto 2
Delay 3
Inverter 2
Convert 2
Goto 6
Convert 1
Goto 1
arg_addr
rst
T_half
CTRL - AUX
Goto 7

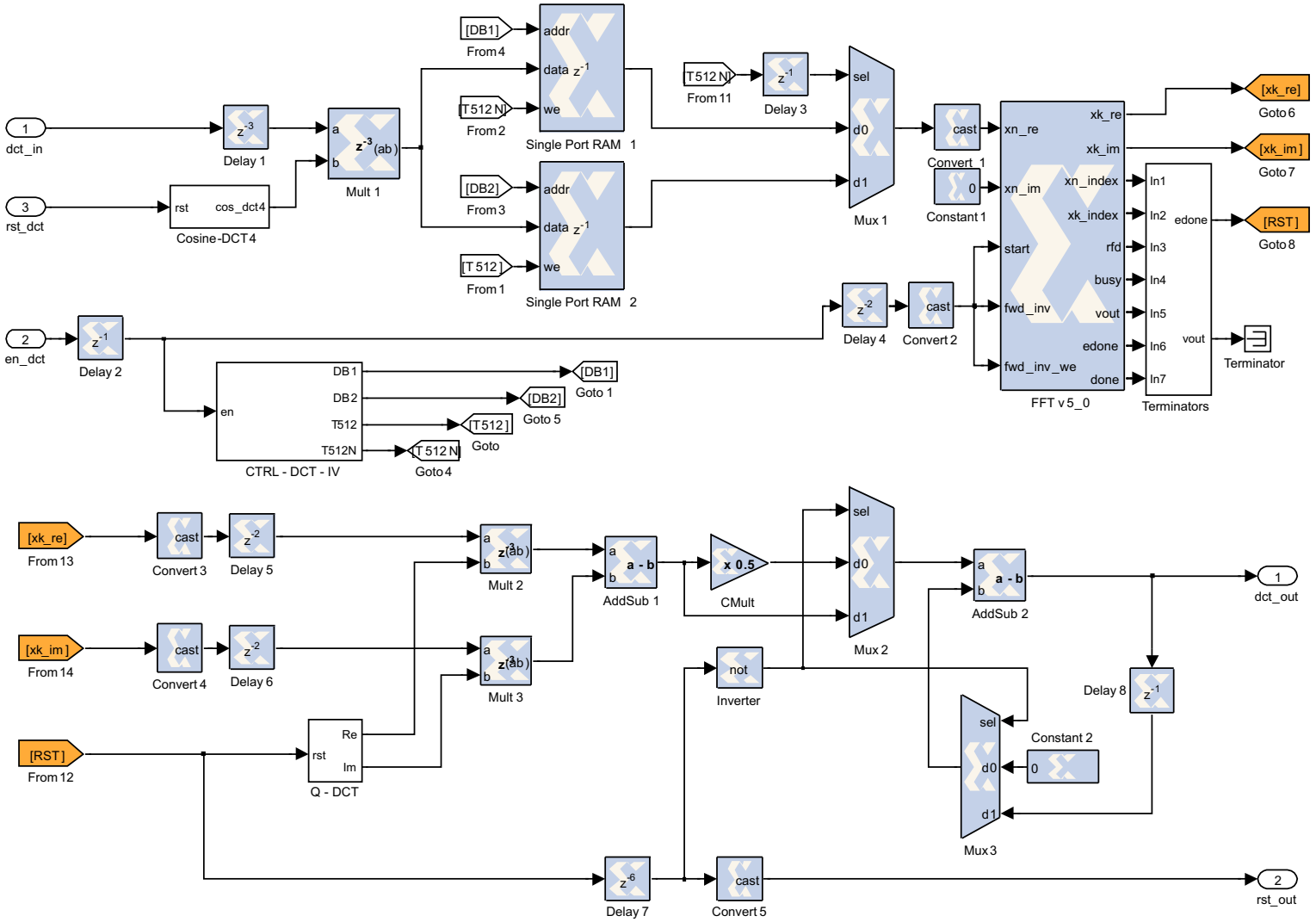

SC0 - TX
SC1 - TX

ELT-II


[B]
From 6
addr
data z-1
we
[A1]
From
RAM 1
in_a
in_b
arg
out_a
out_b
SC1 - RX
z-1024
Delay 3
[A3]
From 5
[B]
From 4
Delay 4
[A2]
From 3
RAM2
Delay 6
sel
d0
d1
Mux
1
signal _in
From 1
[B]
not
Inverter 2
[B]
From 2
not
Inverter 3
SC0 - RX
Delay 5
dct_in
dct_out
1
symbol _out
3
en_dct
en_dct
start_out
2
start_symbol
4
rst_dct
rst_dct
DCT - IV - RX
2
rst_elt 2
arg_addr
rst
T_half
CTRL - AUX
[B]
Goto 1
z-9
Delay 1
[A3]
Goto 3
z-8
Delay 2
cast
Convert 1
[A2]
Goto 2
not
Inverter 1
cast
Convert 2
[A1]
Goto


SC1 - RX
SC0 - RX

DCT-IV


1
dct_in
Delay 1
3
rst_dct
Cosine-DCT4
Mult 1
[DB1]
From 4
[T512 N]
From 2
Single Port RAM 1
[DB2]
From 3
[T 512]
From 1
Single Port RAM 2
T512 N
From 11
Delay 3
Mux 1
Constant 1
Convert 1
FFT v 5_0
Terminators
[xk_re]
Goto 6
[xk_im]
Goto 7
[RST]
Goto 8
Terminator
2
en_dct
Delay 2
Delay 4
Convert 2
CTRL - DCT - IV
[DB1]
Goto 1
[DB2]
Goto 5
[T512]
Goto
[T 512 N]
Goto 4
[xk_re]
From 13
Convert 3
Delay 5
Mult 2
AddSub 1
x 0.5
CMult
Mux 2
AddSub 2
1
dct_out
[xk_im]
From 14
Convert 4
Delay 6
Mult 3
Inverter
Delay 8
Constant 2
Mux 3
[RST]
From 12
Q - DCT
Delay 7
Convert 5
2
rst_out

Estimación de recursos de hardware

Recursos	Requerido		Disponible
	Número	Porcentaje [%]	
Number of Slice Registers	21586	31	69120
Number of Slice LUTs	27435	39	69120
Number of bonded IOBs	66	10	640
Number of Block RAM/FIFO	21	14	148
Number of BUFG/BUFGCTRLs	1	3	32
Number of DSP48Es	56	87	64